High Dynamic Range Low Ripple RSSI for Zero-IF or Low-IF Receivers

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention relates to a received signal strength indicator for a zero intermediate frequency or a low intermediate frequency radio device such as a receiver or transceiver. Such a radio device receives radio frequency signals, and, when a transmit part is also present, also transmits signals. Such a radio device can be a cellular radio device, a cordless telephone, a wireless local area network radio device, a satellite radio device, or any other suitable radio device.

2. DESCRIPTION OF THE RELATED ART

In the US Patent No. 5,603,112, a received signal strength indicator is disclosed. The received signal strength indicator is used for performing signal strength measurements of received radio frequency signals in radio frequency receivers. The received signal strength indicator comprises analog to digital converters for sampling quadrature down modulated signals at an intermediate frequency. Output signals of the analog to digital converters are supplied to respective comparators that compare magnitudes of the quadrature intermediate frequency signals. Based on comparison results, the magnitudes of either the in-phase signal or quadrature signal is supplied to either a divide-by-16 divider, to a divide-by-8 divider, or by a divide-by-4 divider. The in-phase and quadrature signals, and the divided in-phase and quadrature signals are combined in a number of adders,

one of the adders providing the received signal strength indicator signal. Through such a comparison, division, and combining, a scaled combination of approximated magnitudes of in-phase and quadrature down converted quadrature signals is computed, approximating the magnitude of the received vector, the received vector being the square root of the sum of the squared magnitudes of the in-phase and quadrature down converted quadrature signals. Such a computation of an approximation of the magnitude of the received vector, used as a received signal strength indicator signal in the intermediate frequency domain, is complex.

In the US Patent No. 5,338,985, a received signal strength indicator for operation at intermediate frequencies is disclosed. The received signal strength indicator comprises a number of cascaded amplifiers that amplify an intermediate frequency signal. Output signals of the respective amplifiers are rectified, and, after voltage to current conversion, currents representing rectified signals are weightedly added so as to obtain a received signal strength indicator signal. From the last amplifier of the multistage amplifier to the first amplifier, the amplifiers successively run out of their linear region and get into their limiting or clipping range, with an increasing input signal amplitude. Herewith, the resulting received signal strength indicator signal approximates a linear function of the logarithm of the input intermediate frequency signal. The more amplifier stages in the cascade of amplifiers, the better the linear approximation is.

In the US Patent No. 5,978,664, peak detector is disclosed. The peak detector is particularly suitable for measuring the peak value of an RSSI signal formed by a multistage limiting and summing logarithmic amplifier. Reducing a ripple in a combination of a multistage limiting and summing logarithmic amplifier and

peak detector, desirable to get a more reliable received signal strength indicator signal, renders the time response of the combination worse, i.e., the signal undesirably slowly decays after a sudden change in the amplitude of the highly dynamic radio signal to be measured.

On page 62 of the DRAFT Supplement, Part 11, of the IEEE 802.11b standard, operating channels are shown for North American Channel selection in the so-called 2.4 GHz ISM band.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a received signal strength indicator signal at zero intermediate frequency or low intermediate frequency that is simple, that is low ripple, and that has a high dynamic range.

It is another object of the invention to provide a received signal strength indicator that produces a received signal strength indicator signal approximating a linear function of the logarithm of an input signal supplied to the received signal strength indicator.

It is still another object of the invention to provide a received signal strength indicator wherein for a particular modulation type of signals, such as QPSK, signal glitches are avoided.

In accordance with the invention, a method of determining a received signal strength indicator signal from an in-phase signal component and a quadrature signal component of a low intermediate frequency signal that represents a received radio frequency signal, is provided comprising:

determining a first absolute value from said in-phase signal component;

determining a second absolute value from said quadrature signal component; and

summing said first and second absolute values.

The approximately linear function of the logarithm of the input signal is obtained by logarithmically processing of signals, either before or after determining the first and second absolute values.

Preferably, logarithmic processing is performed before determining the first and second absolute values, by a multistage limiter followed by an adder for adding signals produced by the limiter, in both the in-phase and quadrature signal path.

By low pass filtering the added absolute values, signal glitches are avoided.

BRIEF DESCRIPTION OF THE DRAWING

Figure 1 schematically shows a block diagram of a transceiver with a received signal strength indicator according to the invention.

Figure 2 shows a first embodiment of a received signal strength indicator according to the invention.

Figure 3 shows a second embodiment of a received signal strength indicator according to the invention.

Figure 4 shows an absolute signal former.

Figure 5 shows an adder.

Figure 6 shows a multistage limiter and adder.

Throughout the figures the same reference numerals are used for the same features.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figure 1 shows a block diagram of a transceiver 1 as a zero intermediate frequency or low intermediate frequency radio device. Such a radio device can be a time division duplex radio device operating in the so-called 2.4 GHz ISM band, accordance with said IEEE 802.11b standard, or any other suitable radio

device. The transceiver 1 comprises a receive branch Rx and a transmit branch Tx. In another embodiment in which no transmit branch Tx is present, the radio device is a receiver only. The transmit branch Tx comprises a quadrature mixer comprised of filters 2 and 3, mixers 4 and 5, and an adder 6. The adder 6 is coupled to a power amplifier 7. The power amplifier 7 is coupled to an Rx/Tx-switch 8. The Rx/Tx-switch 8 is coupled to an antenna 9. Quadrature transmit signals Tx_I and Tx_Q are generated by a modulator (not shown), and supplied to the filters 2 and 3, respectively. The receive branch Rx comprises a low noise radio frequency amplifier (LNA) 10 that is coupled to the Rx/Tx-switch 8. The LNA 10 amplifies a radio frequency signal RF that is received by the antenna 9. The receive branch Rx further comprises a quadrature down converter that comprises mixers 11 and 12 and channel filters 13 and 14. The transceiver 1 further comprises a frequency synthesizer 15 that generates quadrature local oscillator signals LO_I and LO_Q. The signal LO_I is supplied to the mixers 4 and 11. The signal LO_Q is supplied to the mixers 5 and 12. If the transceiver 1 is a zero intermediate frequency radio device operating in the ISM band, and receiving and transmitting in channel one of the ISM band, the frequency synthesizer 15 is tuned to 2.4 GHz. If the transceiver 1 is a low intermediate frequency radio device operating in the same band and channel, the frequency synthesizer is tuned to a slightly different frequency than 2.4 GHz. The transceiver 1 further comprises a base band circuit 16 with analog to digital converters 17 and 18 for processing down converted quadrature signals Rx_I and Rx_Q, and with a processor 19. The processor 19 comprises non-volatile memory (not shown) with a stored program, and volatile memory (not shown) for storing temporary data. The transceiver 1 further comprises a received signal strength indicator circuit 20 according to the invention that provides a

received signal strength indicator signal RSSI. The signal RSSI is a high dynamic range low ripple signal, at zero-IF or at low IF that resolves the dynamic high range of the received radio frequency signal RF. In a radio device operating in the ISM band, the dynamic range typically is 80 dB. The signal RSSI can be used for controlling functions in the transceiver 1, or to provide signal strength information to a system in which the transceiver operates. The RSSI circuit 20 can be implemented in conventional digital hardware technology, or as a so-called ASIC (Application Specific Integrated Circuit), or as a programmed processor, or any other suitable implementation. In case the RSSI circuit 20 is implemented as a programmed processor, in addition to demodulating sampled signals Rx_I and Rx_Q, the processor performs a computational function to compute the signal RSSI. If needed for analog control function in the transceiver 1, a computed signal RSSI is supplied to a digital to analog converter.

Figure 2 shows a first embodiment of the received signal strength indicator (RSSI) 20 according to the invention. The RSSI 20 comprises a limiter and summer 30 to which the signal Rx_I is supplied, and a limiter and summer 31 to which the signal Rx_Q is supplied. Limited and summed signals are supplied to respective absolute signal formers 32 and 33. Absolute signals are added by an adder 34. Added absolute signals are low pass filtered by low pass filter 35. The low pass filter provides the RSSI signal.

Figure 3 shows a second embodiment of the received signal strength indicator 20 according to the invention. The RSSI 20 comprises absolute signal formers 40 and 41 to which the respective signals Rx_I and Rx_Q are supplied, and further an adder 42 for adding absolute signals. The adder 42 is coupled to a logarithmic signal former 43. The logarithmic signal former 43 is coupled a low pass filter 44 providing the RSSI signal.

Figure 4 shows an absolute signal former comprised of a hard limiter 50 and a multiplier 51. The hard limiter 50 can be a high gain amplifier. A signal V_{IN} appears at the output as a signal $ABS(V_{IN})$.

Figure 5 shows an adder comprised of an operational amplifier 60 with resistors R to provide input signals V_1, V_2, and V_3 to the opamp 60, and a feedback resistor R_f. An output signal of the opamp is $VOUT = -R_f/R.(\Sigma V_i)$, $i = 1, 2, 3$.

Figure 6 shows a multistage limiter and adder comprised of a cascade of differential amplifiers 70 and 71, further differential amplifier stages being indicated by a dashed line. The number of stages is six, for instance. The stage 70 comprises transistors 72 and 73 to which an input signal V_i is supplied. Further shown is a load resistor RL. Similarly, the stage 71 comprises transistors 74 and 75. The signal V_i is supplied to all stages. Through an adder 76, a log limited signal is formed from the amplified signals V_i.

In view of the foregoing it will be evident to a person skilled in the art that various modifications may be made within the spirit and scope of the invention as hereinafter defined by the appended claims and that the invention is thus not limited to the examples provided. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim.